

FDFS2P753AZ

Integrated P-Channel PowerTrench® MOSFET and Schottky Diode -30V, -3A, 115mΩ

Features

- Max $r_{DS(on)}$ = 115mΩ at $V_{GS} = -10V$, $I_D = -3.0A$
- Max $r_{DS(on)}$ = 180mΩ at $V_{GS} = -4.5V$, $I_D = -1.5A$
- $V_F < 0.45V$ @ 2A
 $V_F < 0.28V$ @ 100mA
- Schottky and MOSFET incorporated into single power surface mount SO-8 package
- Electrically independent Schottky and MOSFET pinout for design flexibility
- RoHS Compliant

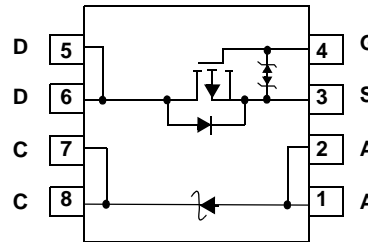
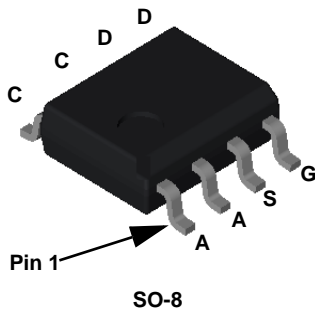


General Description

The FDFS2P753AZ offers a single package solution for DC/DC conversion. It combines an excellent Fairchild's PowerTrench MOSFET with a Schottky diode in an SO-8 package. The MOSFET features a low on-state resistance and an optimized gate charge to achieve fast switching. The independently connected Schottky diode has a low forward voltage drop to minimize power loss. This device is an Ideal DC-DC solution for up to 3A peak load current.

Applications

- DC - DC Conversion



MOSFET Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Rated	Units
V_{DS}	Drain to Source Voltage	-30	V
V_{GS}	Gate to Source Voltage	± 25	V
I_D	Drain Current -Continuous	-3	A
	-Pulsed	-16	
P_D	Power Dissipation	$T_C = 25^\circ C$	W
	Power Dissipation	$T_A = 25^\circ C$ (Note 1a)	
E_{AS}	Single Pulse Avalanche Energy	6	mJ
V_{RRM}	Schottky Repetitive Peak Reverse Voltage	30	V
I_O	Schottky Average Forward Current	2	A
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ C$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	40	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	78	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDFS2P753AZ	FDFS2P753AZ	SO-8	330mm	12mm	2500units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
--------	-----------	-----------------	-----	-----	-----	-------

Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = -250\mu\text{A}$, $V_{GS} = 0\text{V}$	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$, referenced to 25°C		-21		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -24\text{V}$, $V_{GS} = 0\text{V}$ $T_J = 125^\circ\text{C}$			-1 -100	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 25\text{V}$, $V_{DS} = 0\text{V}$			± 10	μA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = -250\mu\text{A}$	-1.0	-2.1	-3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$, referenced to 25°C		5		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -10\text{V}$, $I_D = -3.0\text{A}$ $V_{GS} = -4.5\text{V}$, $I_D = -1.5\text{A}$ $V_{GS} = -10\text{V}$, $I_D = -3.0\text{A}$, $T_J = 125^\circ\text{C}$		69 115 97	115 180 162	m Ω
g_{FS}	Forward Transconductance	$V_{DD} = -5\text{V}$, $I_D = -3.0\text{A}$		6		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -15\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$		330	455	pF
C_{oss}	Output Capacitance			60	110	pF
C_{rss}	Reverse Transfer Capacitance			55	100	pF
R_g	Gate Resistance		$f = 1\text{MHz}$		18	

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -15\text{V}$, $I_D = -3.0\text{A}$, $V_{GS} = -10\text{V}$, $R_{GEN} = 6\Omega$		6	12	ns
t_r	Rise Time			4	10	ns
$t_{d(off)}$	Turn-Off Delay Time			19	34	ns
t_f	Fall Time			15	27	ns
Q_g	Total Gate Charge		$V_{GS} = 0\text{V}$ to -10V	$V_{DD} = -15\text{V}$, $I_D = -3.0\text{A}$	7.9	11.0
Q_g	Total Gate Charge	$V_{GS} = 0\text{V}$ to -4.5V	4.1		5.7	nC
Q_{gs}	Gate to Source Charge		1.3			nC
Q_{gd}	Gate to Drain "Miller" Charge		2.0			nC

Drain-Source Diode Characteristics

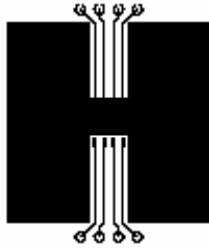
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}$, $I_S = -2.0\text{A}$ (Note 3)		-0.9	-1.2	V
t_{rr}	Reverse Recovery Time	$I_F = -3.0\text{A}$, $di/dt = 100\text{A}/\mu\text{s}$		20	30	ns
Q_{rr}	Reverse Recovery Charge			14	21	nC

Schottky Diode Characteristics

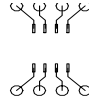
V_R	Reverse Breakdown Voltage	$I_R = 1\text{mA}$	30			V
I_R	Reverse Leakage	$V_R = 10\text{V}$	$T_J = 25^\circ\text{C}$	39	250	μA
			$T_J = 125^\circ\text{C}$	18		mA
V_F	Forward Voltage	$I_F = 100\text{mA}$	$T_J = 25^\circ\text{C}$	225	280	mV
			$T_J = 125^\circ\text{C}$	140		
		$I_F = 2\text{A}$	$T_J = 25^\circ\text{C}$	364	450	
			$T_J = 125^\circ\text{C}$	290		

NOTES:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 78°C/W when mounted on a 0.5 in² pad of 2 oz copper.



b. 135°C/W when mounted on a minimum pad of 2 oz copper.

2. Starting $T_J = 25^\circ\text{C}$, $L = 3 \text{ mH}$, $I_{AS} = -2\text{A}$, $V_{DD} = -27\text{V}$, $V_{GS} = -10\text{V}$.

3. Pulse Test: Pulse Width $< 300\mu\text{s}$, Duty cycle $< 2.0\%$.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

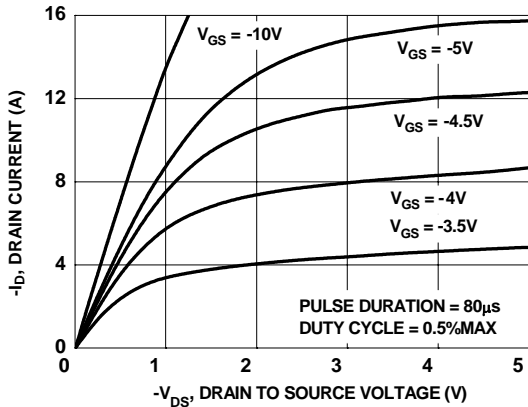


Figure 1. On-Region Characteristics

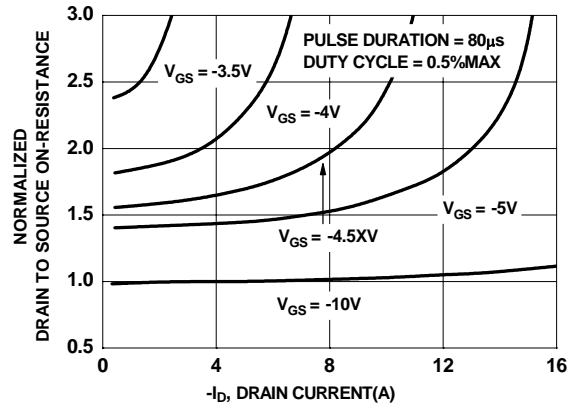


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

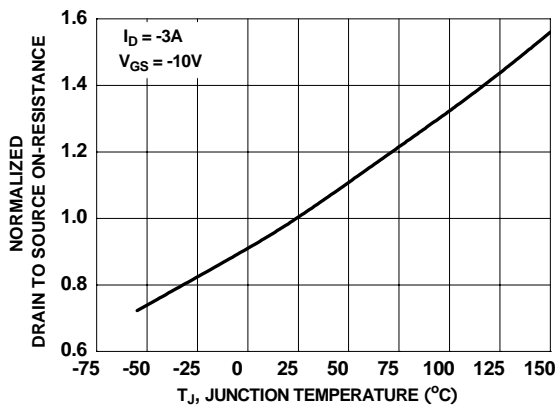


Figure 3. Normalized On-Resistance vs Junction Temperature

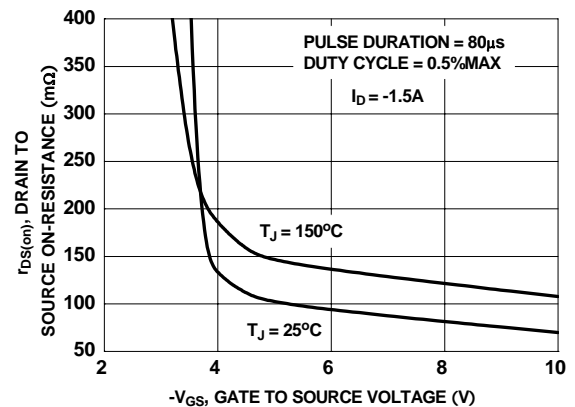


Figure 4. On-Resistance vs Gate to Source Voltage

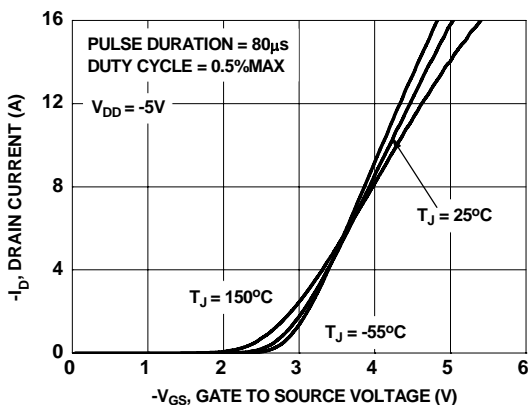


Figure 5. Transfer Characteristics

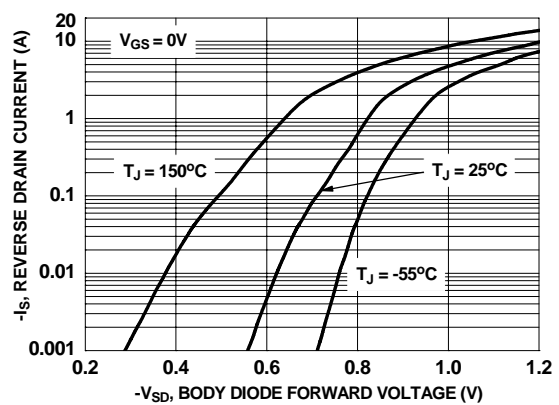


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

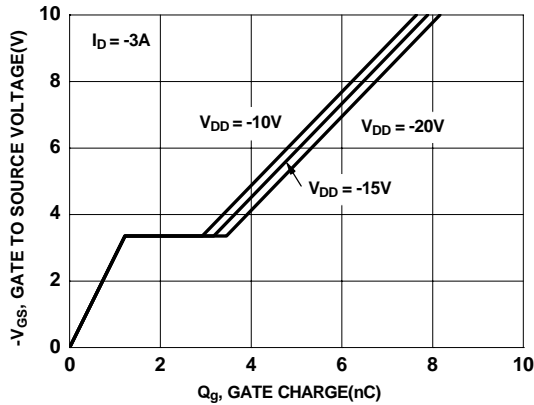


Figure 7. Gate Charge Characteristics

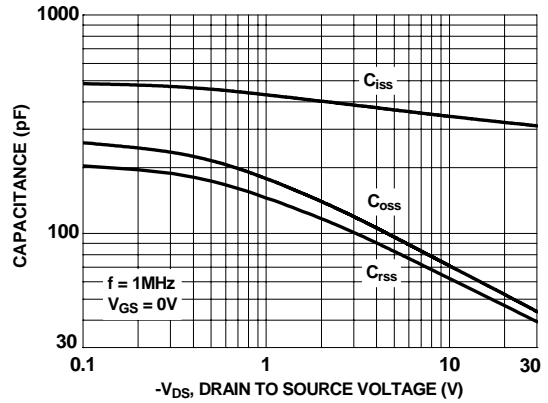


Figure 8. Capacitance vs Drain to Source Voltage

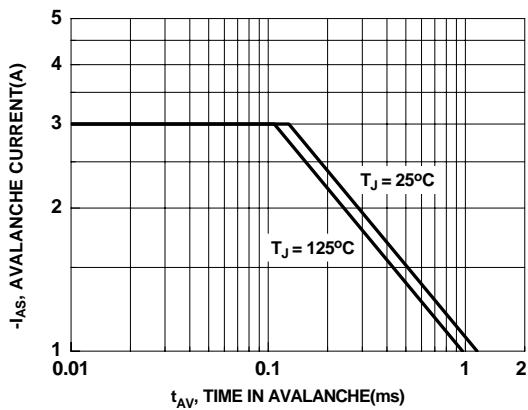


Figure 9. Unclamped Inductive Switching Capability

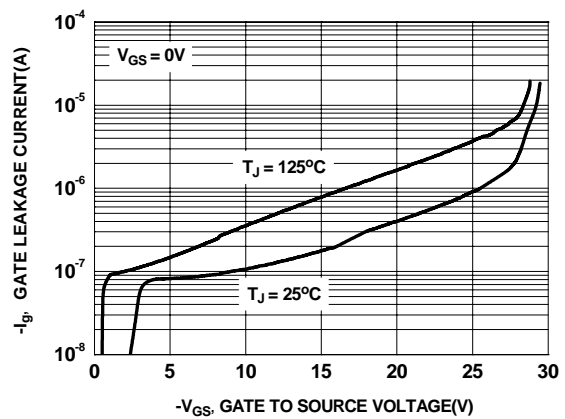


Figure 10. Gate Leakage Current vs Gate to Source Voltage

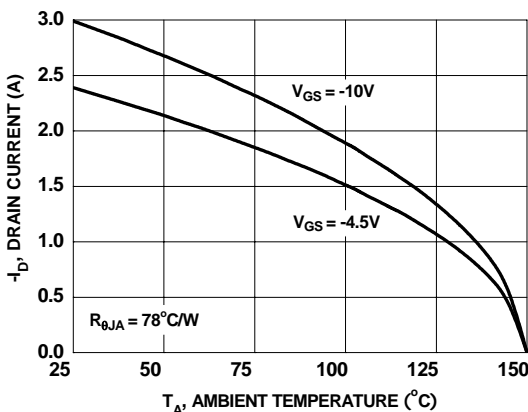


Figure 11. Maximum Continuous Drain Current vs Ambient Temperature

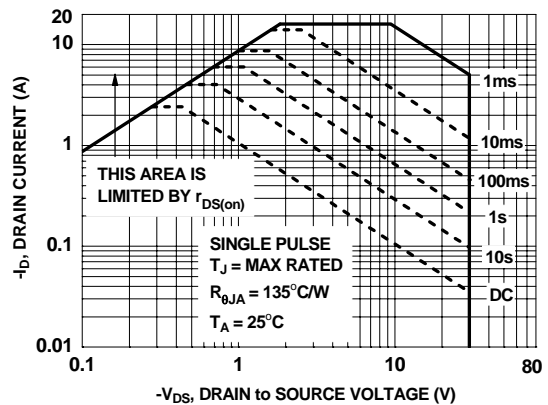


Figure 12. Forward Bias Safe Operating Area

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

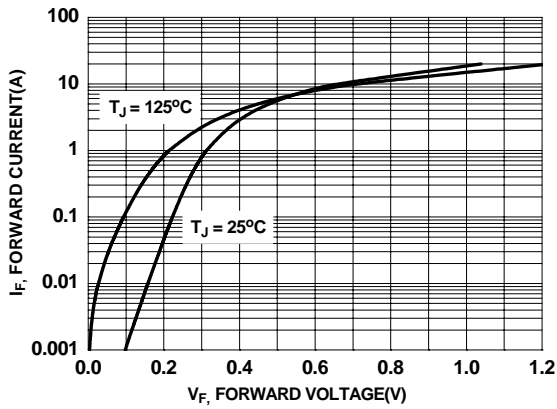


Figure 13. Schottky Diode Forward Voltage

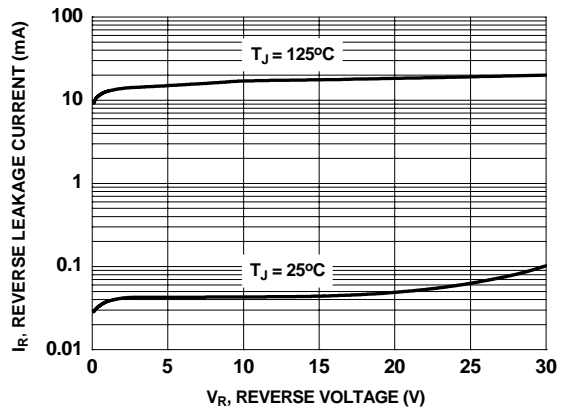


Figure 14. Schottky Diode Reverse Current

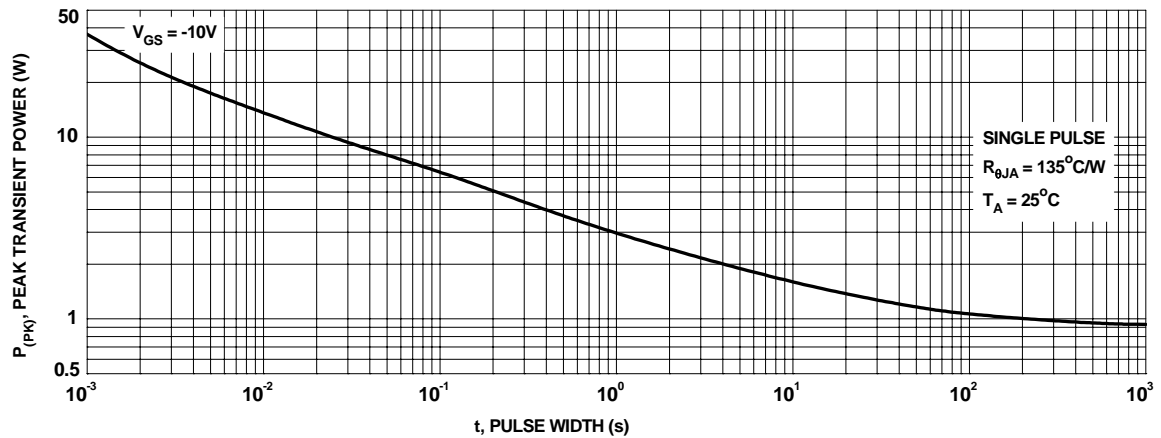


Figure 15. Single Pulse Maximum Power Dissipation

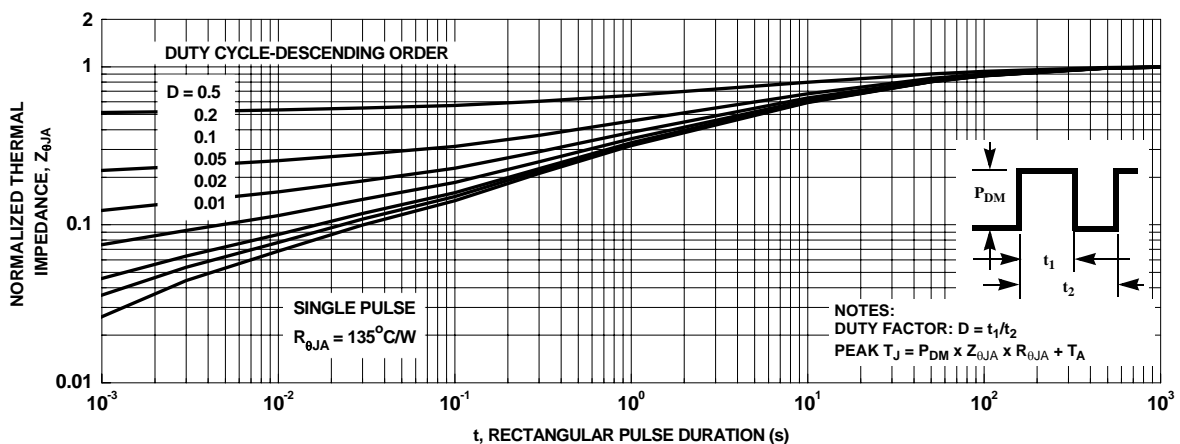


Figure 16. Transient Thermal Response Curve



TRADEMARKS

The following are registered and unregistered trademarks and service marks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx®	Green FPS™ e-Series™	POWEREDGE®	SuperSOT™-8
Build it Now™	GOT™	Power-SPM™	SyncFET™
CorePLUS™	<i>i-Lo</i> ™	PowerTrench®	The Power Franchise®
CROSSVOLT™	IntelliMAX™	Programmable Active Droop™	⏻™
CTL™	ISOPLANAR™	QFET®	TinyBoost™
Current Transfer Logic™	MegaBuck™	QST™	TinyBuck™
EcoSPARK®	MICROCOUPLER™	QT Optoelectronics™	TinyLogic®
FACT Quiet Series™	MicroFEET™	Quiet Series™	TINYOPTO™
FACT®	MicroPak™	RapidConfigure™	TinyPower™
FAST®	Motion-SPM™	SMART START™	TinyPWM™
FastvCore™	OPTOLOGIC®	SPM®	TinyWire™
FPS™	OPTOPLANAR®	STEALTH™	μSerDes™
FRFET®	PDP-SPM™	SuperFET™	UHC®
Global Power Resource SM	Power220®	SuperSOT™-3	UniFET™
Green FPS™	Power247®	SuperSOT™-6	VCX™

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.